



# CALL FOR PAPERS

Abstract Submission Opens—Wednesday, September 17, 2025  
Abstract Submission Closes—Thursday, October 16, 2025 (11:59 pm ET)  
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## Symposium EL12: Recent Innovation in Materials, Processes and Reliability of Advanced Semiconductor Packaging

### MRS—KIM (Korean Institute of Metals and Materials) Joint Symposium

Recent developments in semiconductor technologies for smaller form-factor, high performing multi-function, and more energy saving are strongly driven forward by the advance packaging technologies that realize the 2.xD IC stacking and 3D IC stacking of chiplets. The advanced integration of chiplets is carried out through RDL-interposers, bridges, TSV/TGV, build-up substrates, and more. There are a plethora of advanced materials and processes playing significant roles in the implementation of the chiplet stacking; ultrafine pitch interconnect/dielectrics materials for electrical, thermal, and mechanical integrity and bonding technologies such as micro bump-to-bump bonding, flip chip bonding, bumpless hybrid bonding, including the evaluation of their reliabilities. Flexible hybrid electronics also introduces an additional level of complexity to be handled at the advanced packaging level. This symposium deals with the advanced materials and processes for interconnects, dielectrics, interfaces, bonding, reliabilities for advanced semiconductor packaging technologies, for the sake of sharing new ideas, outcomes, and future research in the relevant research and industry communities.

### Topics Will Include:

- Conductor and dielectric materials for high density interconnects, interposers, bridges and buildup substrates
- Thermal dissipation/interface materials including thermal management of advanced package architectures
- Material deposition processes for advanced packages, such as electroplating, ALD, CVD, PVD, molding
- Interconnect bonding technologies such as thermo-compression bonding and bumpless hybrid bonding (W2W, C2W, and C2C), including planarization (CMP, electropolishing) for chiplet stacking
- Mechanical, electrical, thermal reliability of materials for advanced packaging, such as wafer warpage, electro/thermo/stress-migration, thermal shock/fatigue

### Invited Speakers Include:

- **Byeong-Soo Bae**, Korea Advanced Institute of Science and Technology, Republic of Korea
- **Griselda Bonilla**, IBM Research, USA
- **Chih Chen**, National Yang Ming Chiao Tung University, Taiwan
- **Jungwan Cho**, Sungkyunkwan University, Republic of Korea
- **Peter Czurratis**, PVA TePla Analytical Systems GmbH, Germany
- **Reinhold Dauskardt**, Stanford University, USA
- **Elvira Fortunato**, Universidade Nova de Lisboa, Portugal
- **Takafumi Fukushima**, Tohoku University, Japan
- **Julius Hallstedt**, Excillum, Sweden
- **Subramanian Iyer**, University of California, Los Angeles, USA
- **Koen Kennes**, imec, Belgium
- **Hak-Sung Kim**, Hanyang University, Republic of Korea
- **Erica Lilleodden**, Fraunhofer IWMS Halle, Germany
- **Amit Marathe**, Google Inc., USA
- **Jun Mizuno**, National Cheng Kung University, Taiwan
- **Thomas Moffat**, National Institute of Standards and Technology, USA
- **Stephane Moreau**, CEA-LETI, France
- **Ganesh Subbarayan**, Purdue University, USA
- **Tiwei Wei**, University of California, Los Angeles, USA
- **Bongyoung Yoo**, Hanyang University, Republic of Korea
- **Ill You**, Seoul National University, Republic of Korea

### Symposium Organizers

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